IN THE CLAIMS:

Please cancel claims 1-22 and add new claims 23-40 as provided herein.

1-22. (Canceled)

23. (New) A semiconductor memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of static memory cells each including a first, second, third, fourth, fifth, and sixth transistors; and

a first and second power lines, feeding operating voltage to said plurality of memory cells and formed of metal layers,

wherein said first power line is coupled to sources of said first and second transistors,

wherein said second power line is coupled to sources of said third and fourth transistors,

wherein gates of said fifth and sixth transistors are coupled to said word lines,

wherein source and drain regions of said fifth and sixth transistors are formed inside a semiconductor substrate,

wherein said second power line is formed in a layer between a substrate surface of said semiconductor substrate and a layer forming said first power line,

wherein channel regions, source and drain regions of said first and second transistors are formed by depositing three poly-silicon layers above the substrate surface,

wherein vertical sides of said three poly-silicon layers, which surfaces are vertical against said substrate surface, are totally surrounded by a gate layer having a dioxide layer inbetween, and

wherein said layer forming said second power line is formed between said three poly-silicon layers and said substrate surface.

24. (New) The memory device according to claim 23,

wherein said three poly-silicon layers includes a first, second, and third poly-silicon layers, and

wherein said first and second transistors are formed by steps of:

depositing the first poly-silicon layer which forms said drain regions,

depositing the second poly-silicon layer above said first poly-silicon layer, which forms said channel regions,

depositing the third poly-silicon layer above said second poly-silicon layer, which forms said source regions,

etching said first, second, and third poly-silicon layers to form columns,

forming said dioxide layer around said vertical sides, and

depositing said gate layer around said dioxide layer.

25. (New) The memory device according to claim 24,

wherein during the etching step, a mask covers a surface of said third poly-silicon layer which is parallel with said substrate surface, and said mask is removed before said layer forming said first power line is formed.

26. (New) The memory device according to claim 24,

wherein said plurality of word lines are formed in a layer between said substrate surface and said layer forming said second power line.

27. (New) The memory device according to claim 24, further comprising:

a peripheral circuit including a row and column decoder,

wherein transistors forming said peripheral circuit includes vertical transistors having currents flowing through channel regions thereof in a vertical direction which is vertical against the substrate surface.

28. (New) The SRAM device according to claim 23, wherein the first, second transistors are arranged in a level different from a level containing the third, fourth transistors.

29. (New) The SRAM device according to claims 28, wherein the transistors located in different levels are selectively connected to each other via at least one vertical interconnect.

30. (New) The SRAM device according to claim 29, wherein said at least one vertical interconnect cross links with at least one of a horizontal interconnect, the first power line, and the second power line, each of which is parallel with the substrate surface.

31. (New) The SRAM device according to claim 23, wherein the semiconductor substrate is made of single crystal Si.

32. (New) A semiconductor memory device comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of static memory cells each including a first, second, third, fourth, fifth, and sixth transistors; and

a first and second power lines, feeding operating voltage to said plurality of memory cells and formed of metal layers,

wherein said first power line is coupled to sources of said first and second transistors,

wherein said second power line is coupled to sources of said third and fourth transistors,

wherein gates of said fifth and sixth transistors are coupled to said word lines,

wherein channel regions, source and drain regions of said fifth and sixth transistors are formed inside a semiconductor substrate such that currents flow via said channel regions aligning in a first direction,

wherein said second power line is formed in a layer between a substrate surface of said semiconductor substrate and a layer forming said first power line,

wherein channel regions, source and drain regions of said first and second transistors are formed by depositing three poly-silicon layers above the substrate surface such that currents flow via said channel regions aligning in a second direction which crosses said first direction at an angle greater than zero degree and smaller than 90 degrees,

wherein aligning sides of said three poly-silicon layers, which surfaces are parallel with said second direction, are totally surrounded by a gate layer having a dioxide layer inbetween, and

wherein said layer forming said second power line is formed between said three poly-silicon layers and said substrate surface.

33. (New) The memory device according to claim 32,

wherein said three poly-silicon layers includes a first, second, and third poly-silicon layers, and

wherein said first and second transistors are formed by steps of:

depositing the first poly-silicon layer which forms said drain regions,

depositing the second poly-silicon layer above said first poly-silicon layer, which forms said channel regions,

depositing the third poly-silicon layer above said second poly-silicon layer, which forms said source regions,

etching said first, second, and third poly-silicon layers to form columns,

forming said dioxide layer around said vertical sides, and

depositing said gate layer around said dioxide layer.

34. (New) The memory device according to claim 33,

wherein during the etching step, a mask covers a surface of said third poly-silicon layer which is parallel with said substrate surface, and said mask is removed before said layer forming said first power line is formed.

35. (New) The memory device according to claim 33,

wherein said plurality of word lines are formed in a layer between said substrate surface and said layer forming said second power line.

36. (New) The memory device according to claim 33, further comprising:

a peripheral circuit including a row and column decoder,

wherein transistors forming said peripheral circuit includes vertical transistors having currents flowing through channel regions thereof in a vertical direction which is vertical against the substrate surface.

37. (New) The SRAM device according to claim 32, wherein the first, second transistors

are arranged in a level different from a level containing the third, fourth transistors.

38. (New) The SRAM device according to claims 37, wherein the transistors located in different levels are selectively connected to each other via at least one vertical interconnect.

39. (New) The SRAM device according to claim 38, wherein said at least one vertical interconnect cross links with at least one of a horizontal interconnect, the first power line, and the second power line, each of which is parallel with the substrate surface.

40. (New) The SRAM device according to claim 32, wherein the semiconductor substrate is made of single crystal Si.